Design of a Dedicated Miller-opAmp

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Overview

1.Design Plan

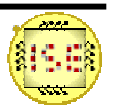
--Calculation according to Allen/D. Holberg, ***CMOS Analog Circuit Design***, Oxford Uni.Press, 1987

2.Simulation Circuits

3.Layout and Post Layout Simulation

4.Results

5.Conculsion



Design Goals

Specifications

•0.35µm Austria Microsystems technology

•Design a 2 stage opAmp adjusted for high speed readout application

	Targeted values
Open Loop Gain	> 70 dB
Gain Bandwidth	10 MHz
Phase Margin	> 65°
Settling Time	< 1 µ s
Slew Rate	> 30 V/ µ s
Offset Voltage	< 10 µV
Input CMR	+/- 1 V
Output Swing	+/- 1 V
CMRR	> 80 dB
Power Dissipation	minimum
Load Capacitance	5p F
Load Resistance	100k Ω

Design Plan

Compensation capacitance:

$C_c > 0.22 C_L$ $\Longrightarrow$ $C_c > 1.1pF$

tail current:

$I_5 = SR * C_c$ $\Longrightarrow$ $I_5 = 33$ uA

Transistor M3,M4:

$$S_3 = \frac{W_3}{L_3} = \frac{I_5}{K'_3\left[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)\right]^2} \geq 1$$

$\Longrightarrow$ **$S_3 = S_4 = 6$**

Transistors M1 , M2:

$$g_{m1} = GB \cdot C_C \Rightarrow S_1 = S_2 = \frac{g_{m2}^{\ 2}}{K_2' I_5}$$

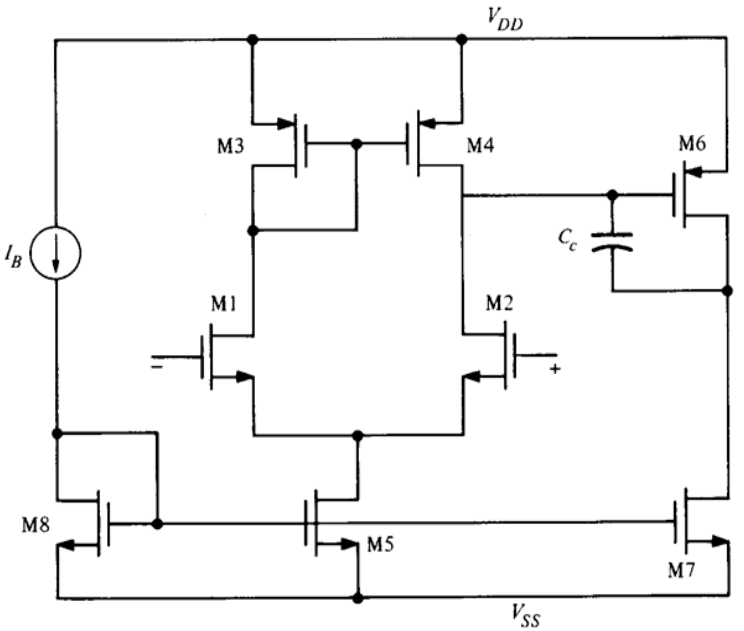
$\Longrightarrow$ **$S_1 = S_2 = 1$**

Transistor M5:

$$V_{DS5}(sat) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100mV$$

$$S_5 = \frac{2I_5}{K_5'\left[V_{DS5}(sat)\right]^2}$$

$\Longrightarrow$ **$S_5 = 2$**



Design Plan

Transistor M6:

$$S_6 = \frac{g_{m6}}{K_6' V_{DS6}(sat)}$$

⇨ **S6=40**

Transistor M7:

$$I_6 = \frac{g_{m6}^{\ 2}}{2K_6' V_{DS6}(sat)}$$

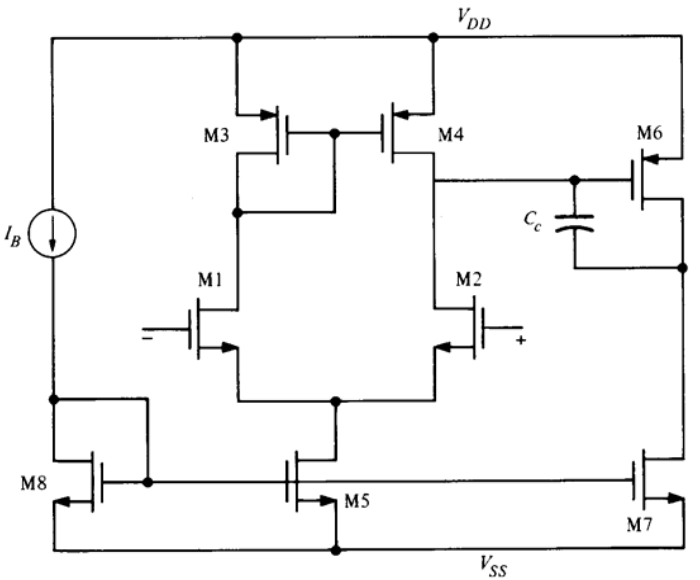
$$S_7 = \frac{I_6}{I_5} S_5$$

⇨ **S7=7**

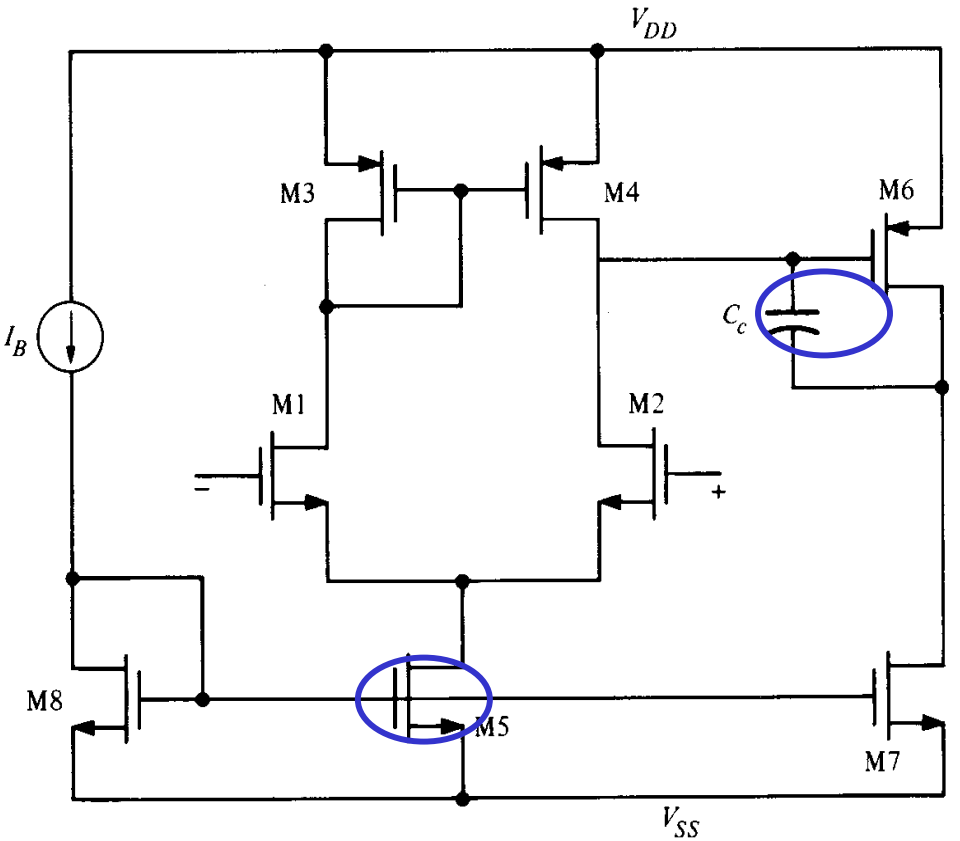
gain and power dissipation:

$$A_V = \frac{2(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3) I_6(\lambda_6 + \lambda_7)} \quad \Rightarrow \quad \textbf{Av=67.1dB}$$

$$P_{diss} = (I_6 + I_5)(V_{DD} - V_{SS}) \quad \Rightarrow \quad \textbf{Pdiss=1.7 mW}$$



Design Plan



Cc=500fF ,SR=164.2 V/ μ s, PM=40 °
Cc=1.5pF ,SR=60.37 V/ μ s ,PM=65 °

Cc=500fF ,Open Loop Gain=72.4dB
Cc=1.5pF ,Open Loop Gain=72.4dB

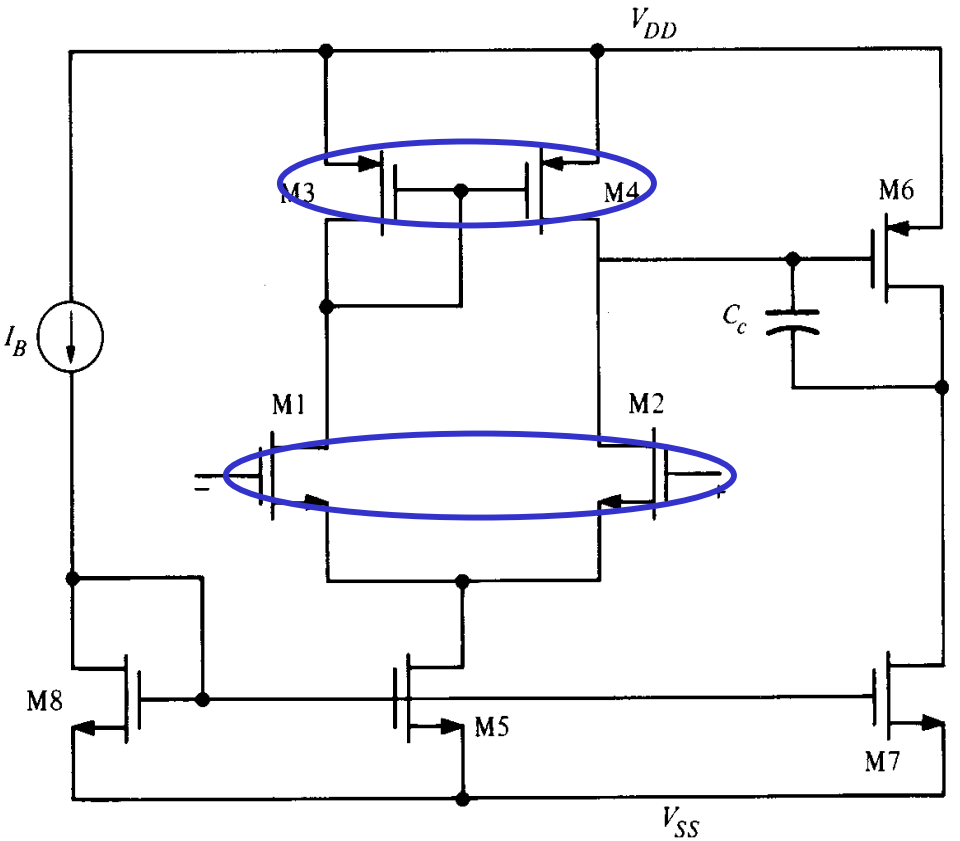
Decrease Cc will increase the SR,but also decrease PM. Cc doesn't change the open loop gain.

S_5=16u SR=60.37 V/ μ s, PM=54.63 °
S_5=32u SR=121.27 V/ μ s ,PM=85 °

S_5=16u Open Loop Gain=72.4dB
S_5=32u Open Loop Gain=27.28dB

Increase S_5 will increase the SR and PM,but decrease the open loop gain alot

Design Plan



S_1=4u ,SR=60.37V/ μ s, Open Loop Gain =72.44dB
PM=65°

S_1=8u, SR=60.59 V/ μ s, Open Loop Gain =75.52dB
PM=56.6°

Increase S1,S2 will increase Open Loop Gain but decrease PM.S_3,S_4 doesn't change the Slew Rate much

S_3=12.5u, Open Loop Gain=72.44 dB, PM=65 °

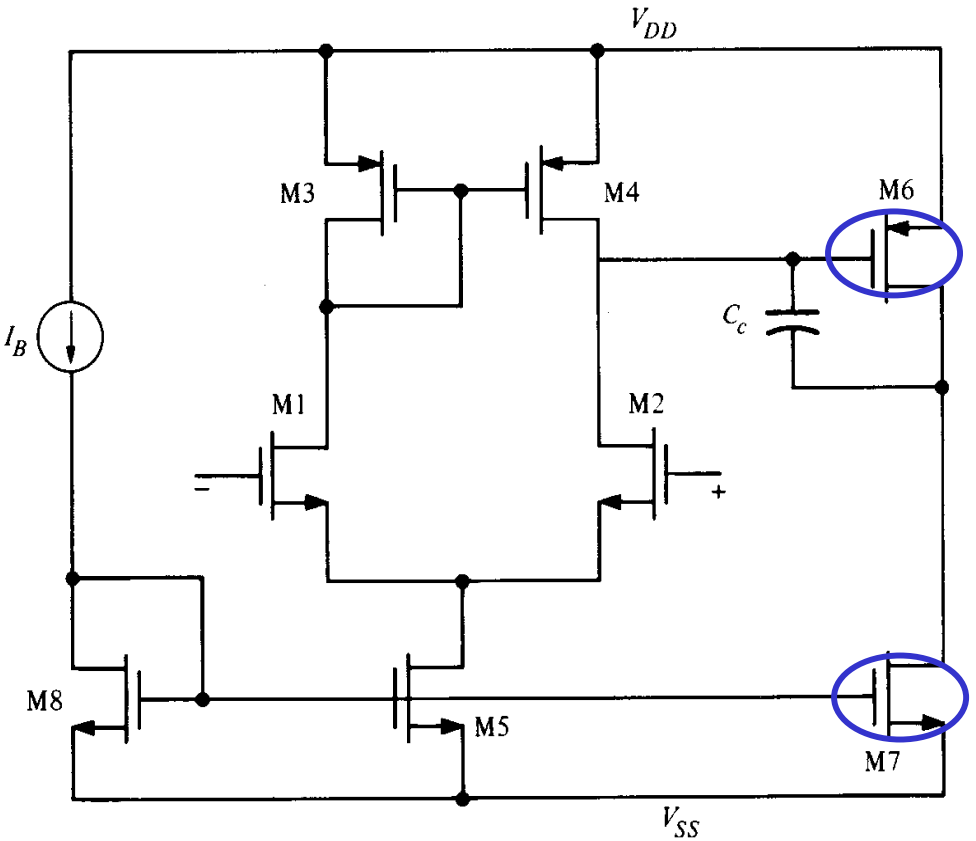
S_3=25u, Open Loop Gain=33.41 dB ,PM=85 °

S_3=12.5u, SR=60.37V/ μ s

S_3=25u, SR=60.68

Increase S_3,S_4 will decrease Open Loop Gain,but increase the PM.S_3,S_4 doesn't change the Slew Rate much

Design Plan



S_6=75u, SR=59.6 V/ μ s, Open Loop Gain=30.4dB
S_6=150u, SR=60.4 V/ μ s ,Open Loop Gain=72.4dB

S_6=75u ,PM=85.3 °
S_6=150u ,PM=65 °

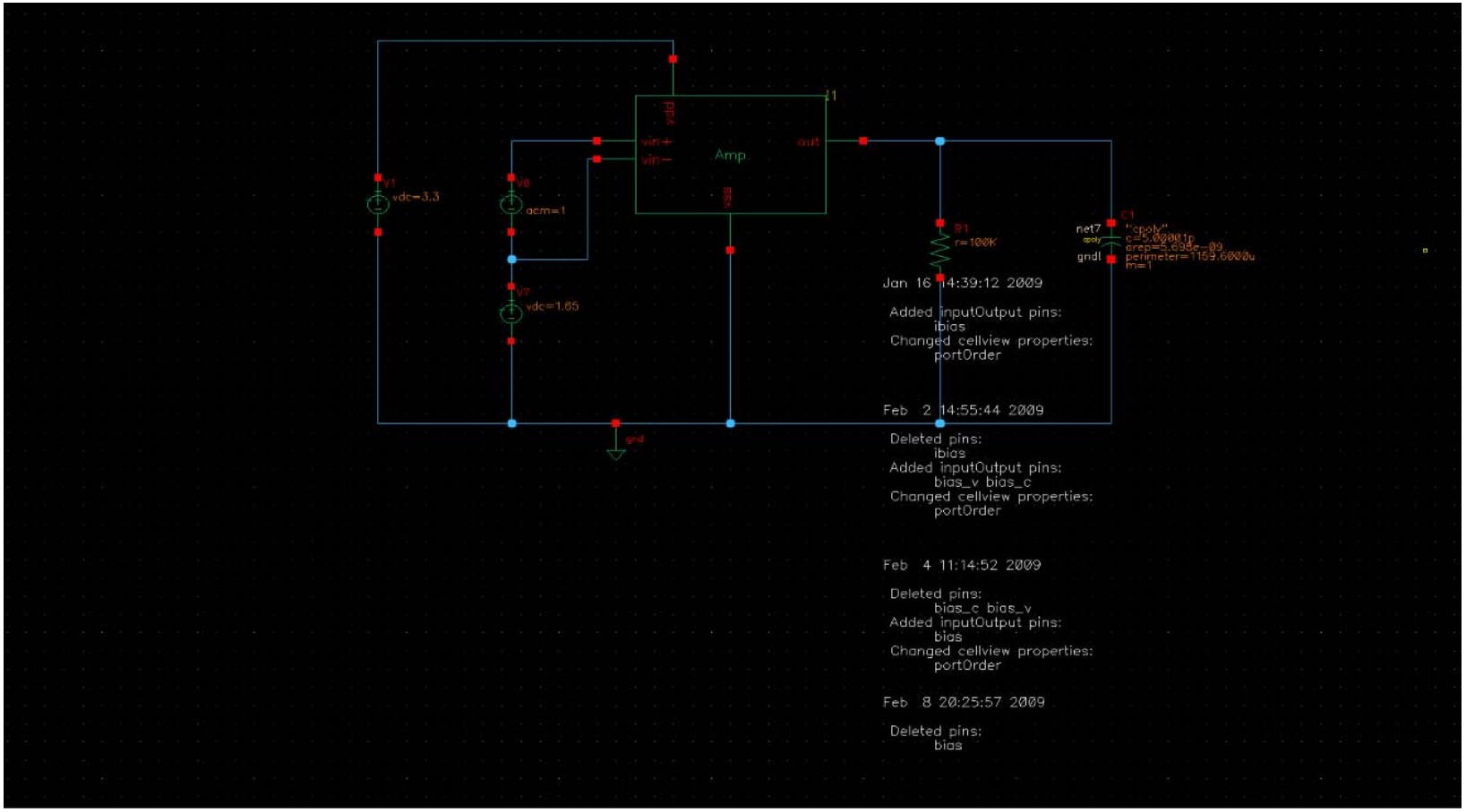
S_7=50u Open Loop Gain=32.4dB,PM=82 °
S_7=95.2u Open Loop Gain=72.4dB, PM=65 °

S_6=50u , SR=60.3 V/ μ s
S_6=95.2u , SR=60.4 V/ μ s

IncreaseS_6,S_7 will increase Open Loop Gain,decrease the PM,they will not change SR much

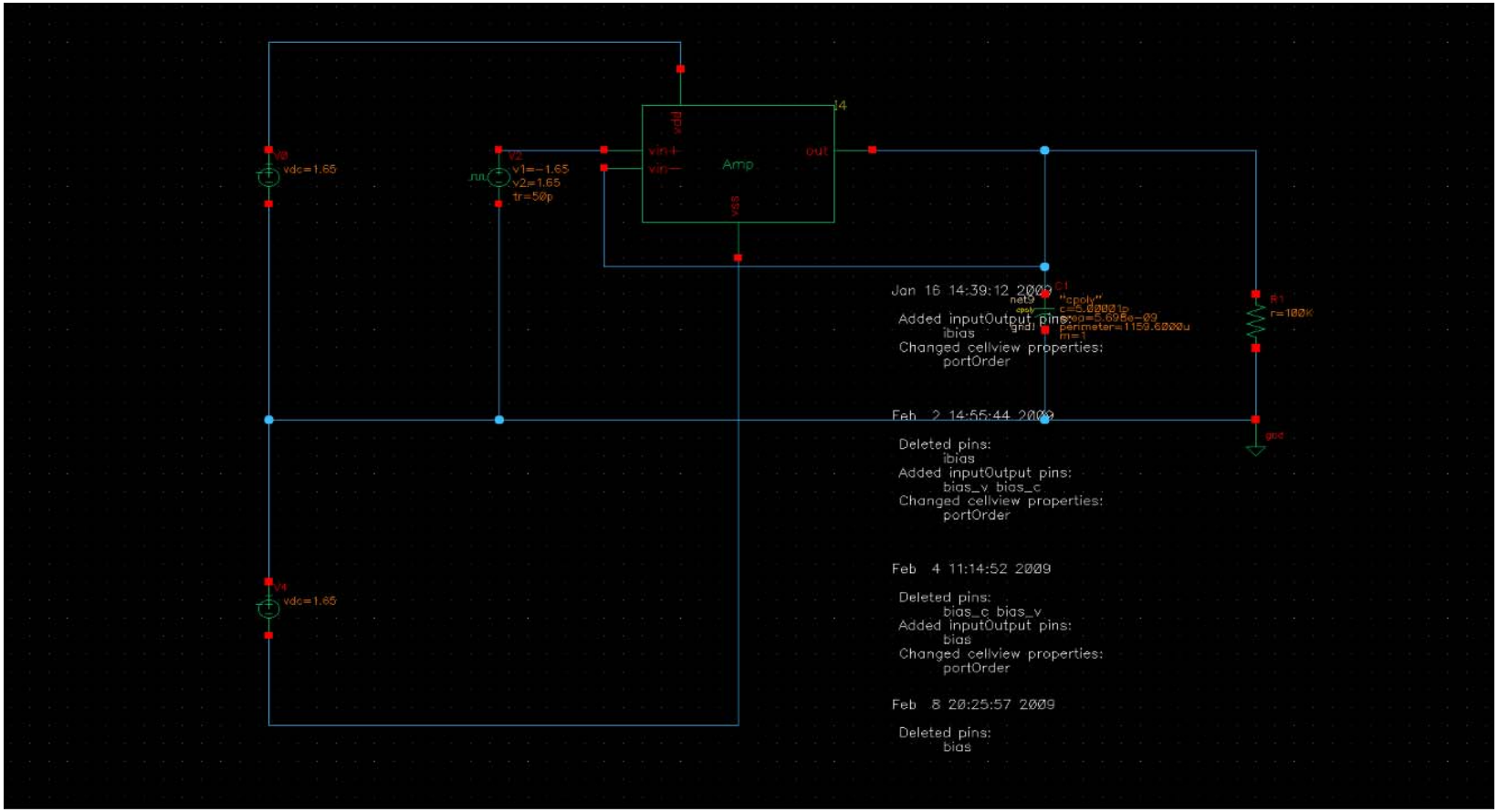
OpAmp Simulation Circuit

OpAmp Open loop Gain ,Gain Bandwidth ,Phase Margin Simulation Circuit



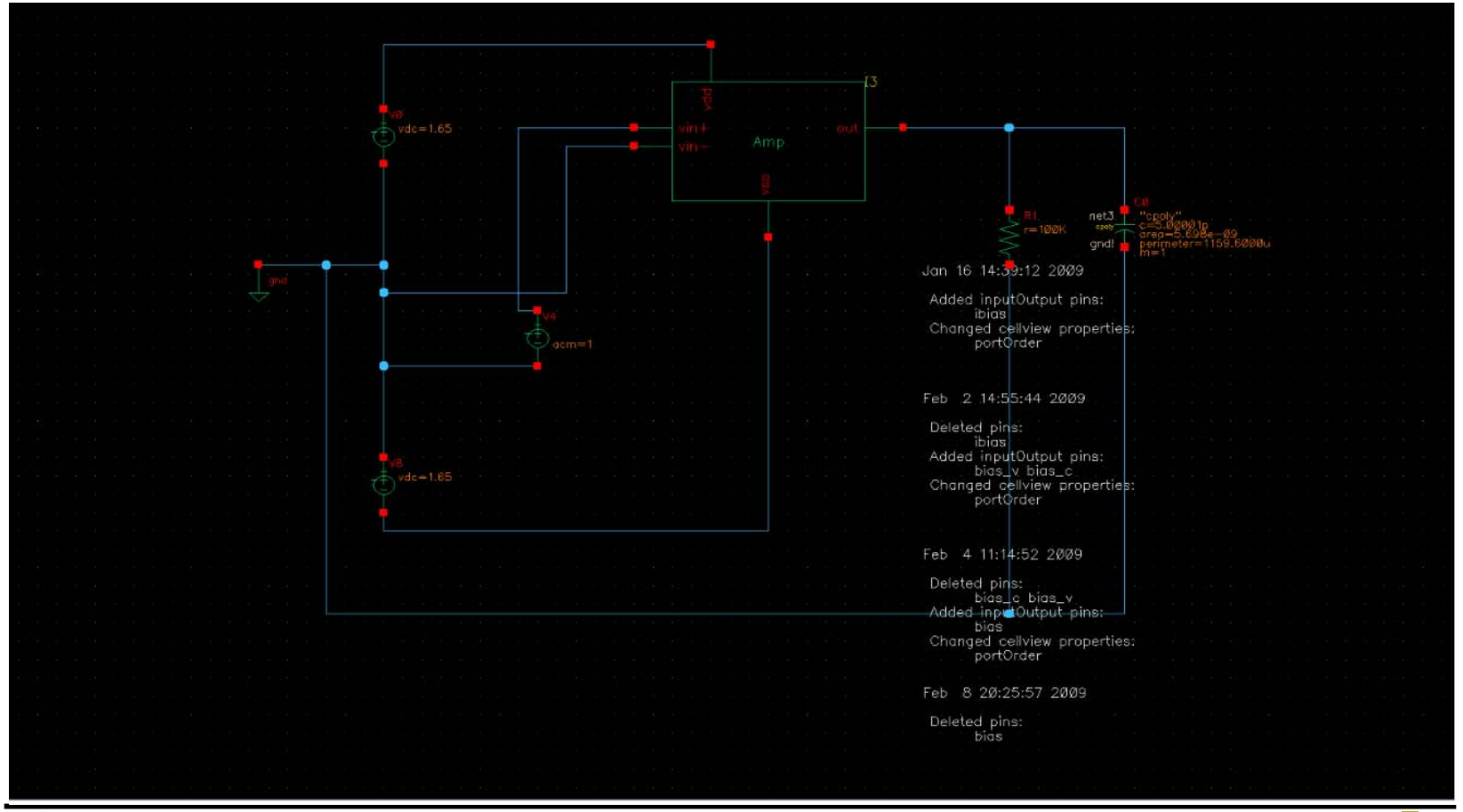
OpAmp Simulation Circuit

OpAmp Slew Rate,Settling Time Simulation Circuit



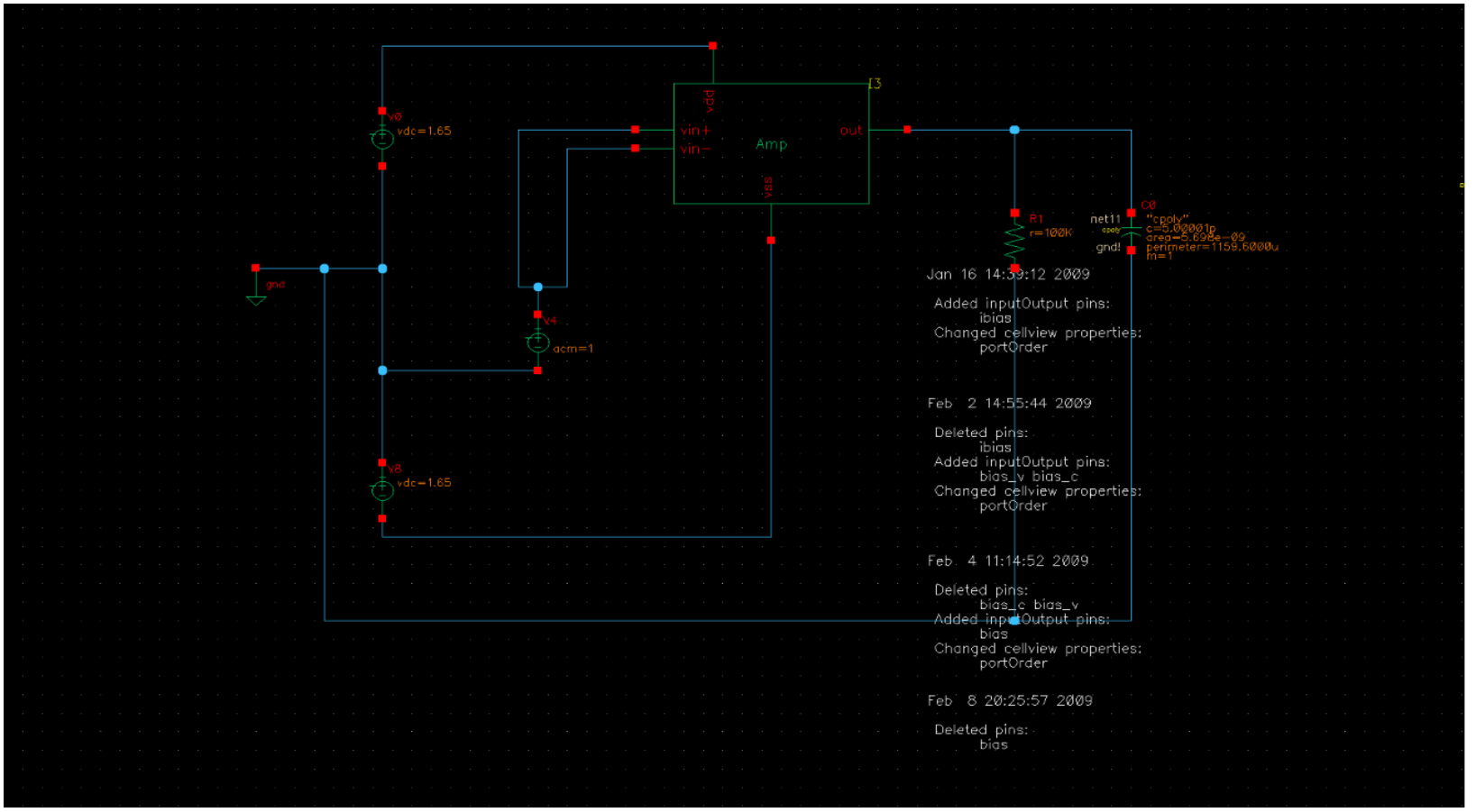
OpAmp Simulation Circuit

OpAmp Differential Mode Gain Simulation Circuit



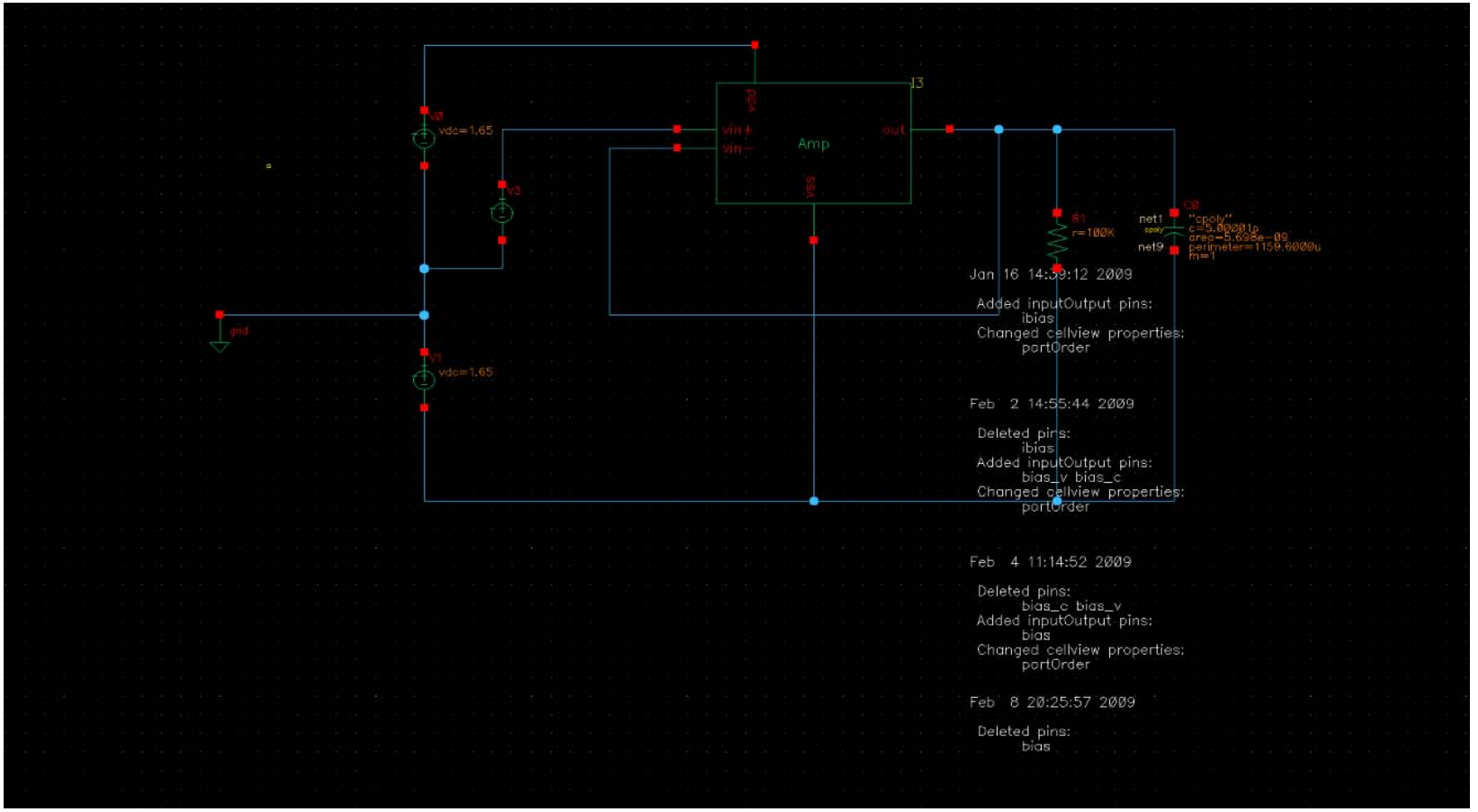
OpAmp Simulation Circuit

OpAmp Common Mode Gain Simulation Circuit



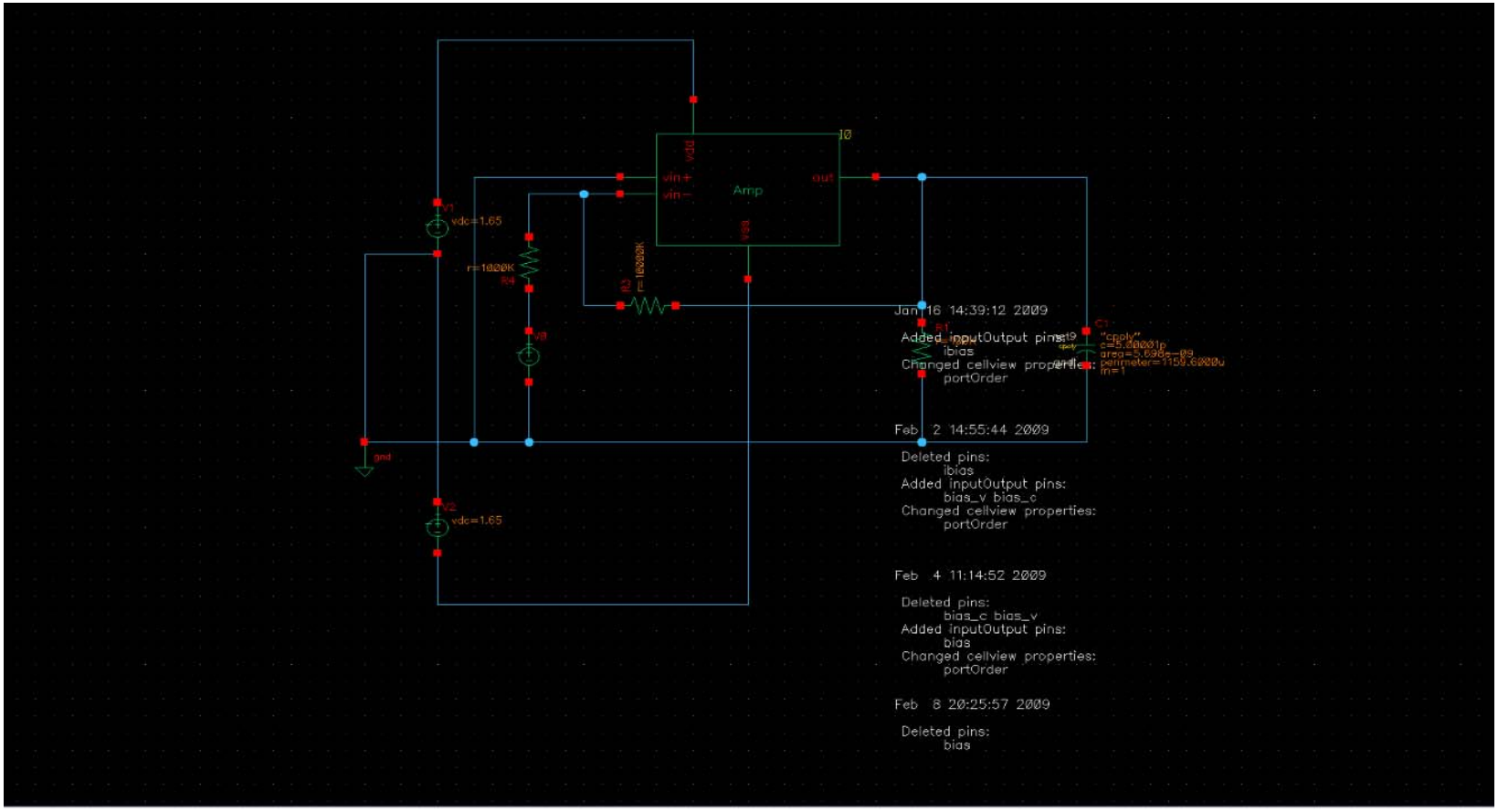
OpAmp Simulation Circuit

OpAmp Input CMR Simulation Circuit



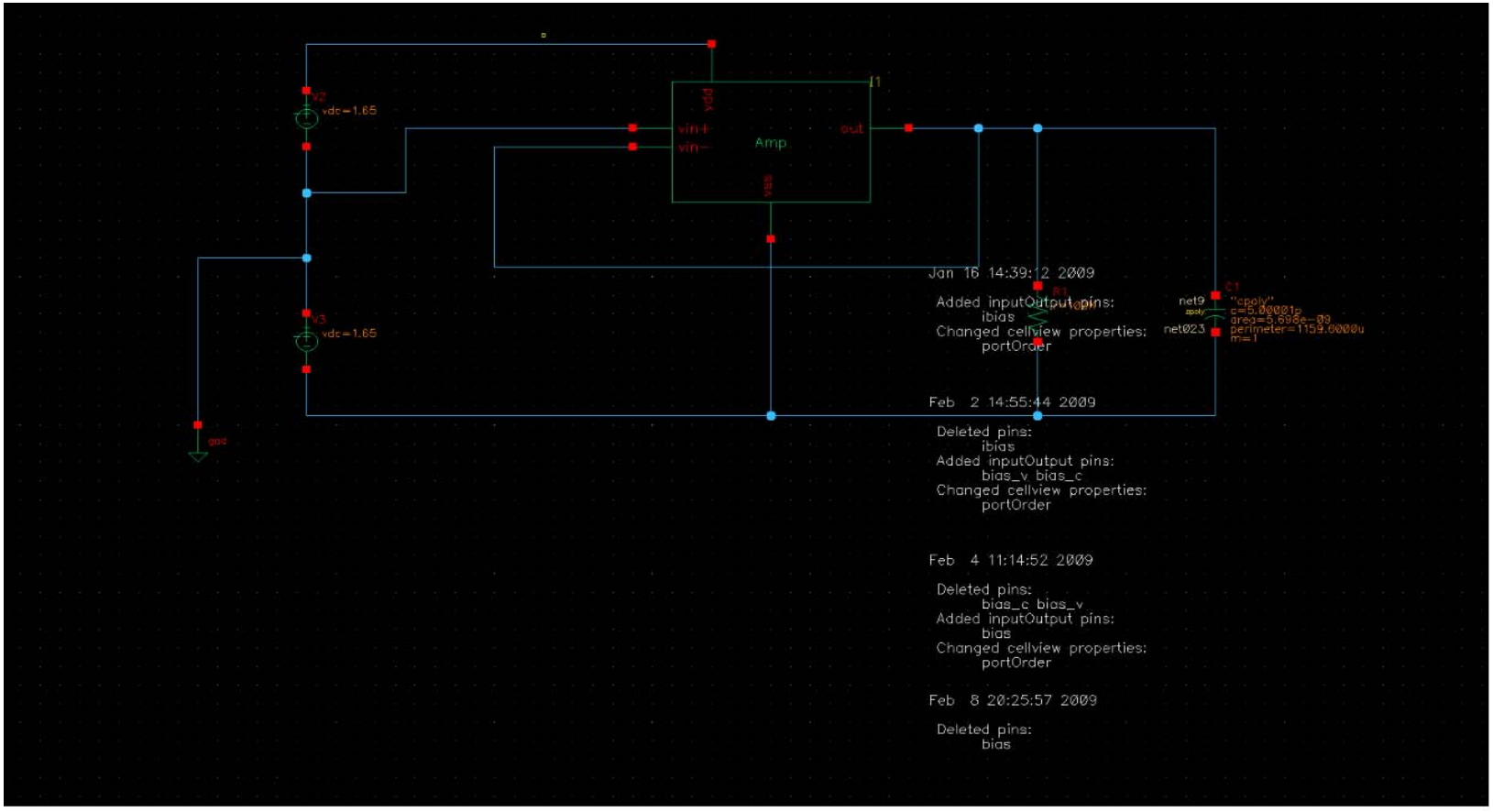
OpAmp Simulation Circuit

OpAmp Output Swing Simulation Circuit



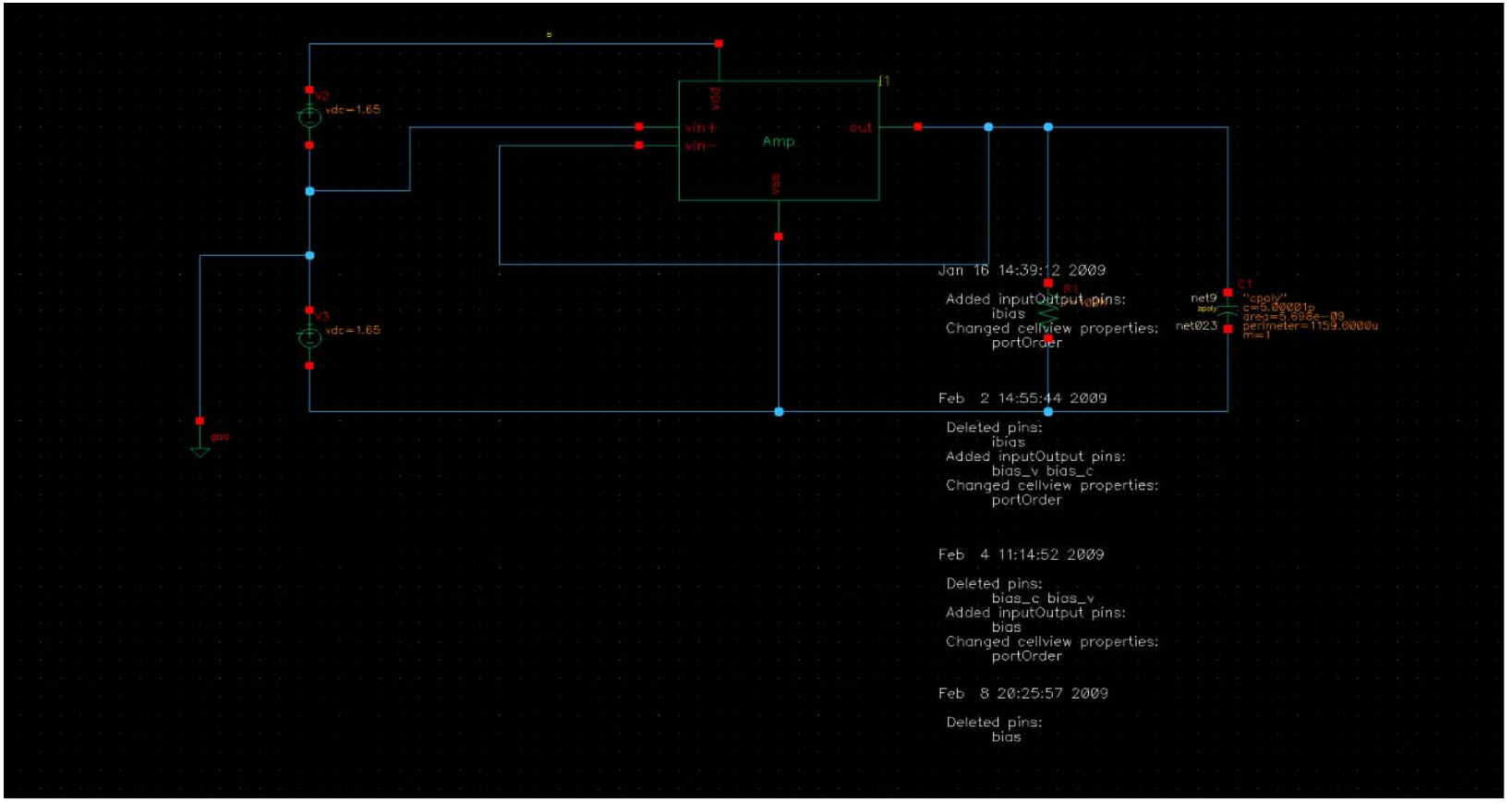
OpAmp Simulation Circuit

OpAmp Offset Voltag Simulation Circuit

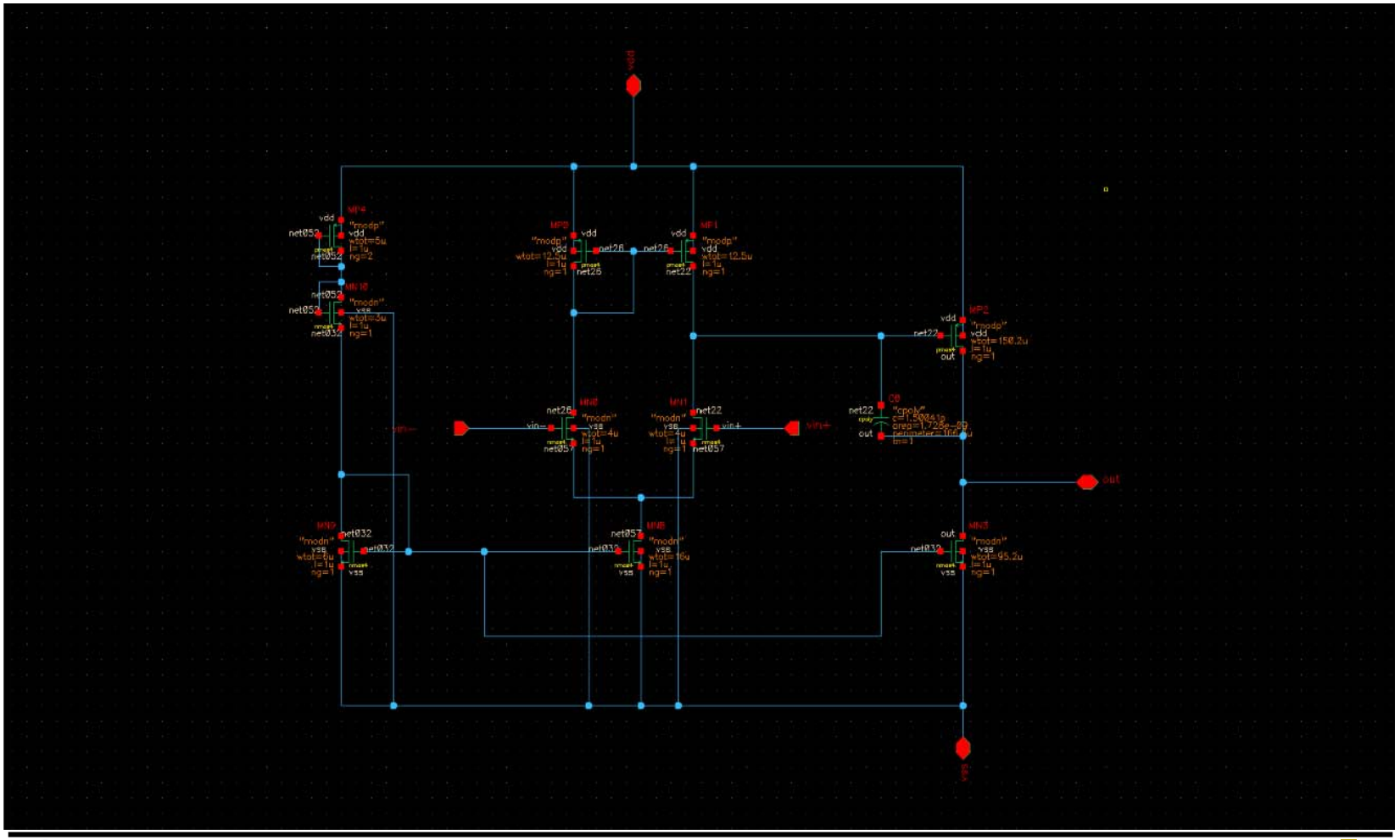


OpAmp Simulation Circuit

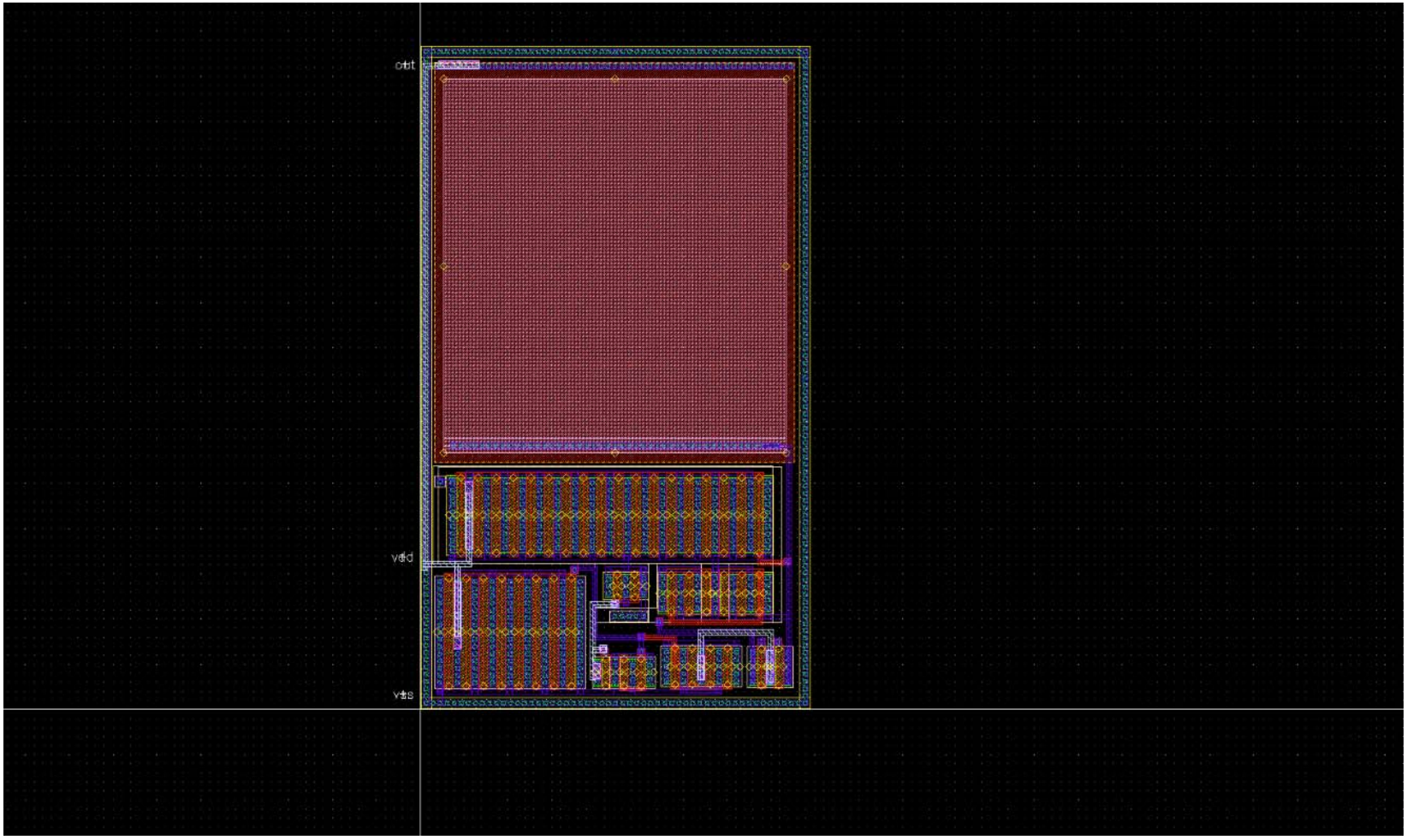
OpAmp Power Dissipation Simulation Circuit



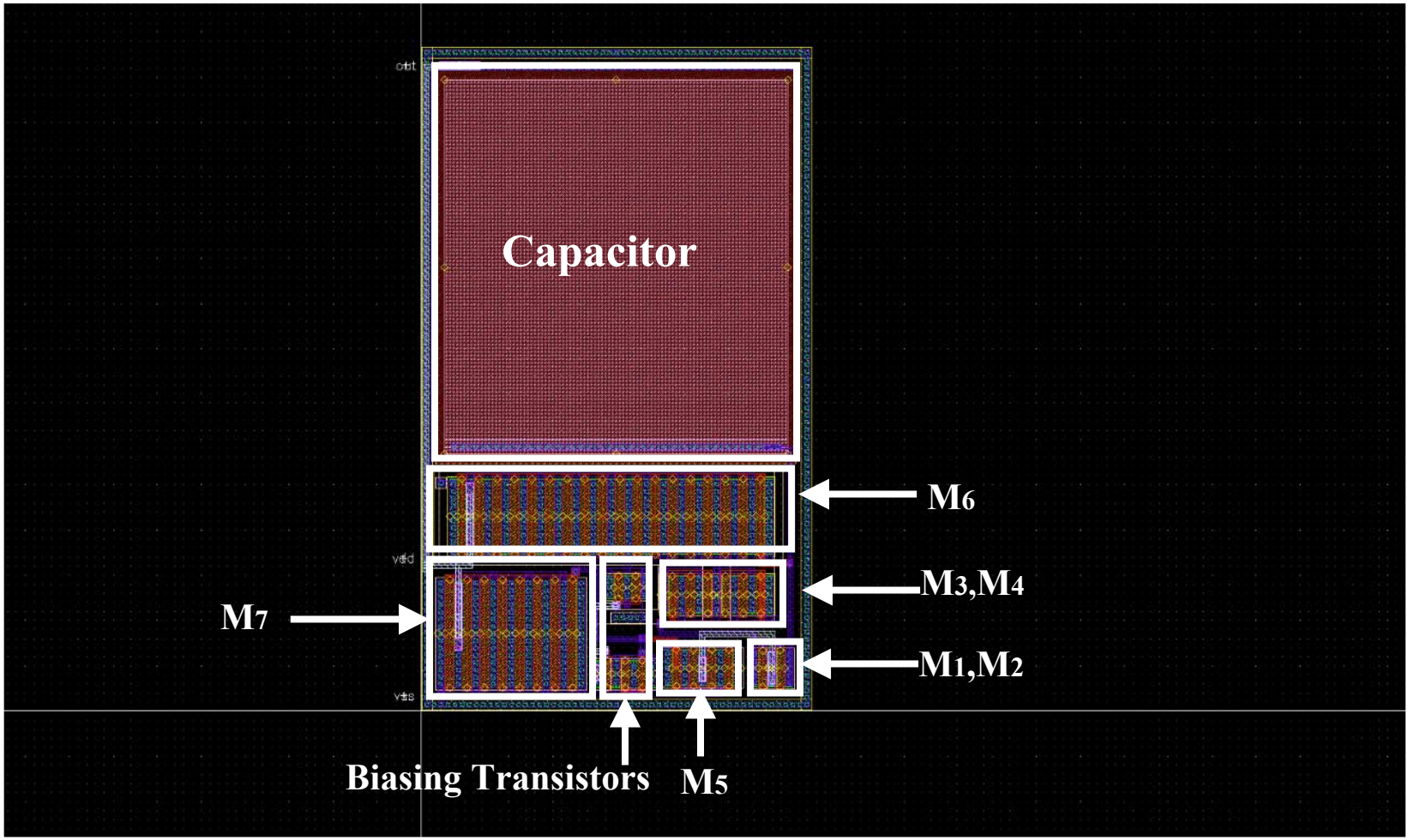
OpAmp Schematic Design



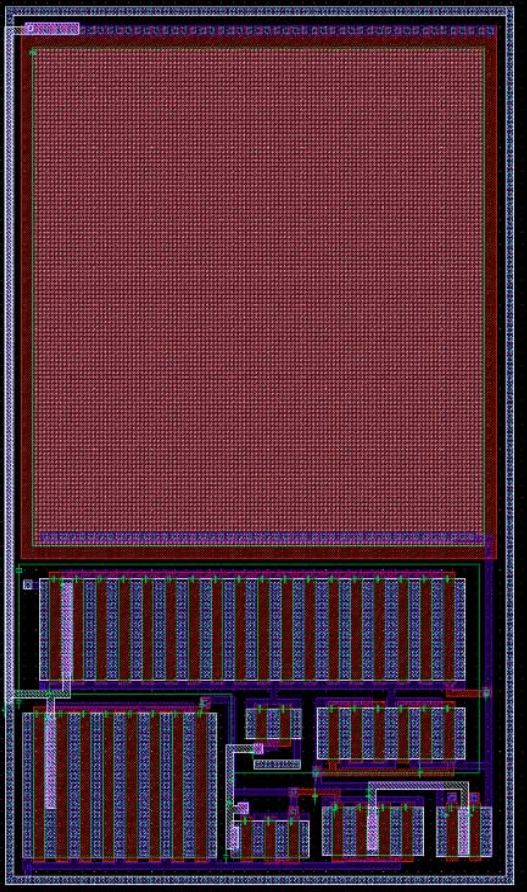
OpAmp Layout Design



OpAmp Layout Design



OpAmp Analog- Extracted View



OpAmp LVS Check

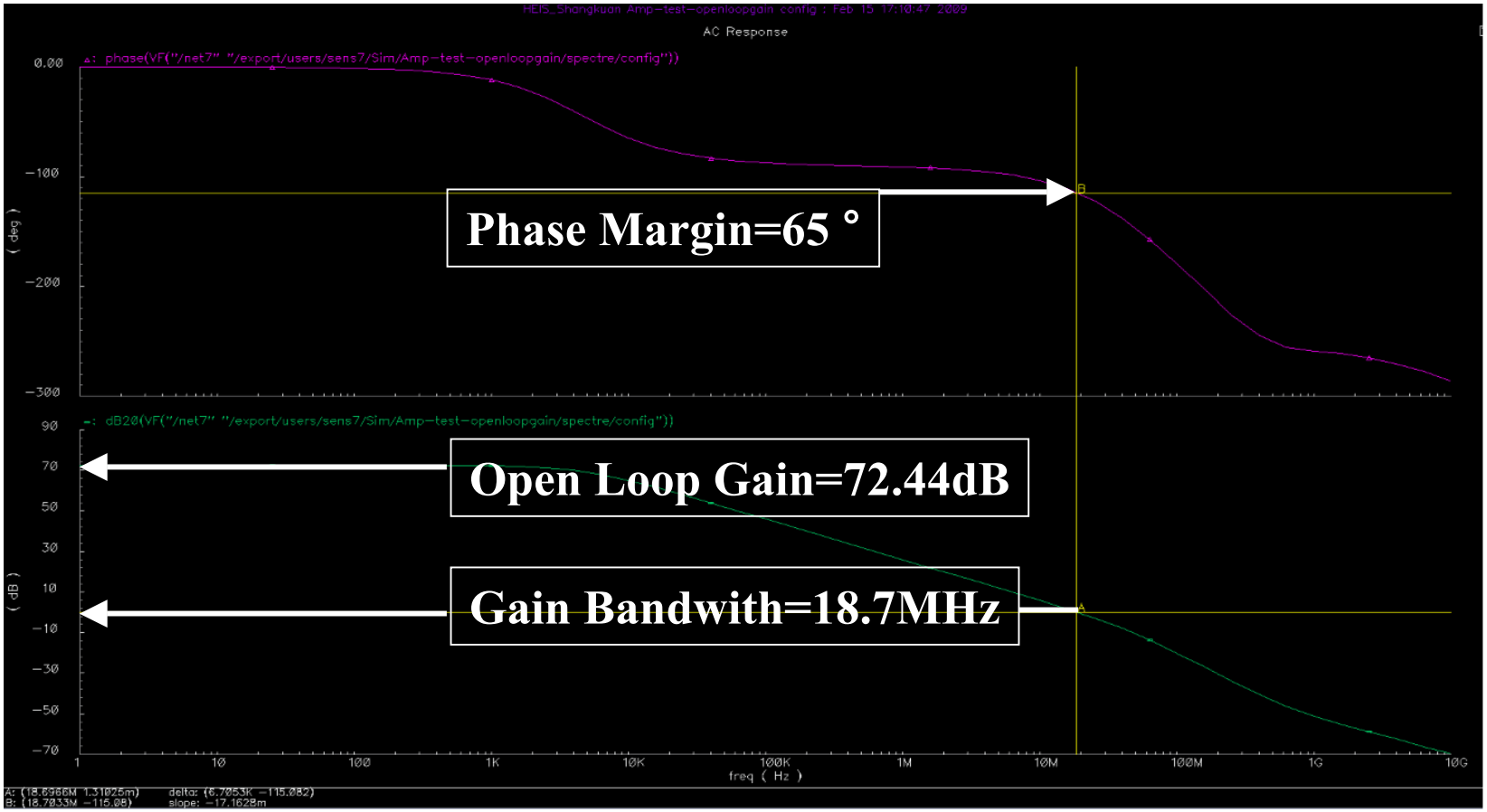
/export/users/sens7/LVS/si.log

File Help 127

```
Warning: Unknown device "rpoly1" on a permuteDevice command.
Warning: Unknown device "lat3" on a permuteDevice command.
Warning: Unknown device "vert15" on a permuteDevice command.
Warning: Unknown device "vert10" on a permuteDevice command.
Warning: Unknown device "vert5" on a permuteDevice command.
Warning: Unknown device "pmosm4" on a permuteDevice command.
Warning: Unknown device "nmosmb4" on a permuteDevice command.
Warning: Unknown device "nmosm4" on a permuteDevice command.
Warning: Unknown device "nmosh6" on a permuteDevice command.
Warning: Unknown device "nmosb4" on a permuteDevice command.
Warning: Unknown device "ng" on a permuteDevice command.
Warning: Unknown device "cvar" on a permuteDevice command.
Warning: Unknown device "csandvt" on a permuteDevice command.
Warning: Unknown device "zd2sm24" on a permuteDevice command.
Warning: Unknown device "pd" on a permuteDevice command.
Warning: Unknown device "nwd" on a permuteDevice command.
Warning: Unknown device "nd" on a permuteDevice command.

The net-lists match.

                          layout  schematic
                             instances
        un-matched              0       0
        revired                 0       0
        size errors             0       0
        pruned                  0       0
        active                 44      11
        total                  44      11

                               nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                 10      10
        total                  10      10

                          terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5
End comparison:       Feb  9 20:42:17 2009


Comparison program completed successfully.
```

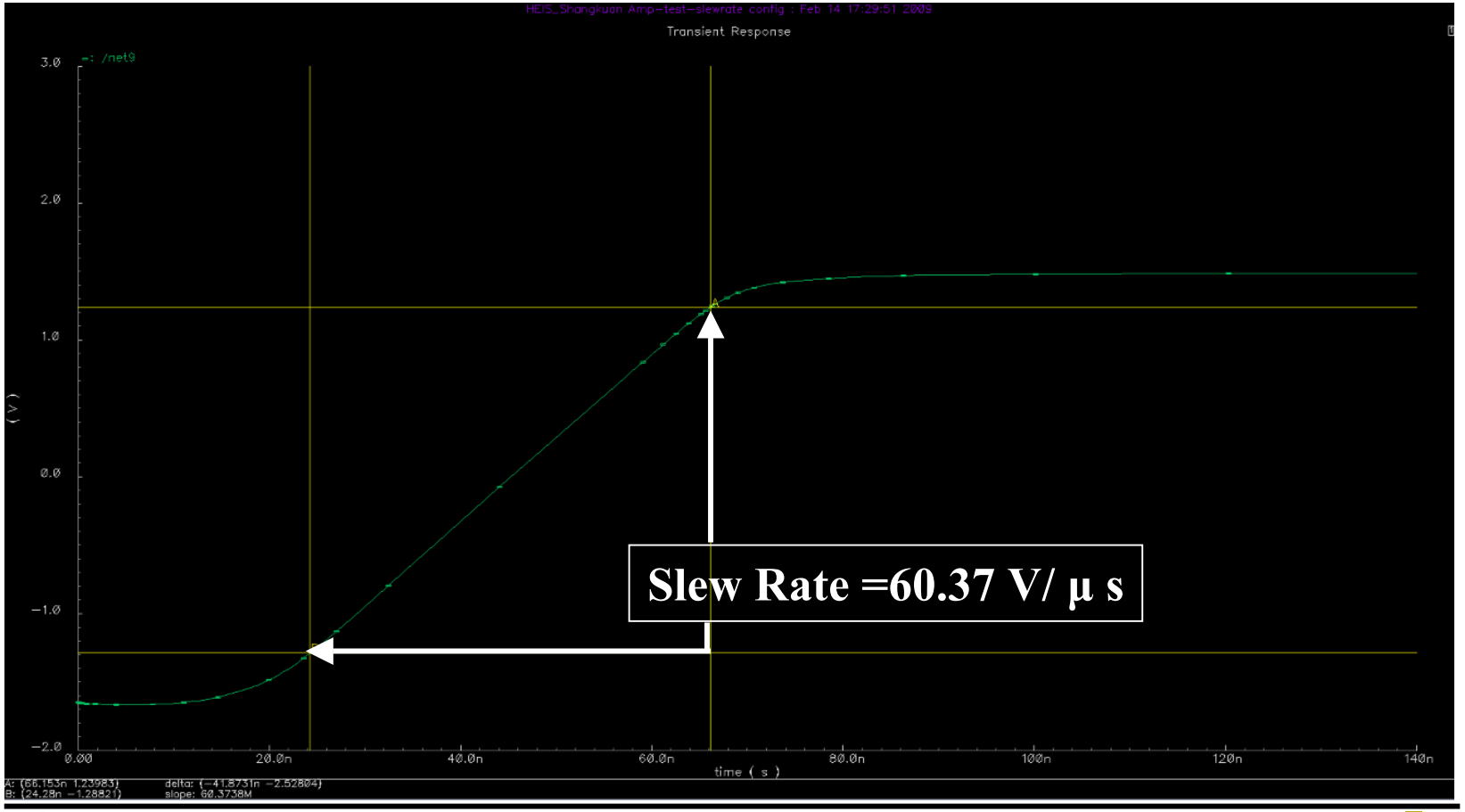
OpAmp Post Layout Simulation

Bode plot



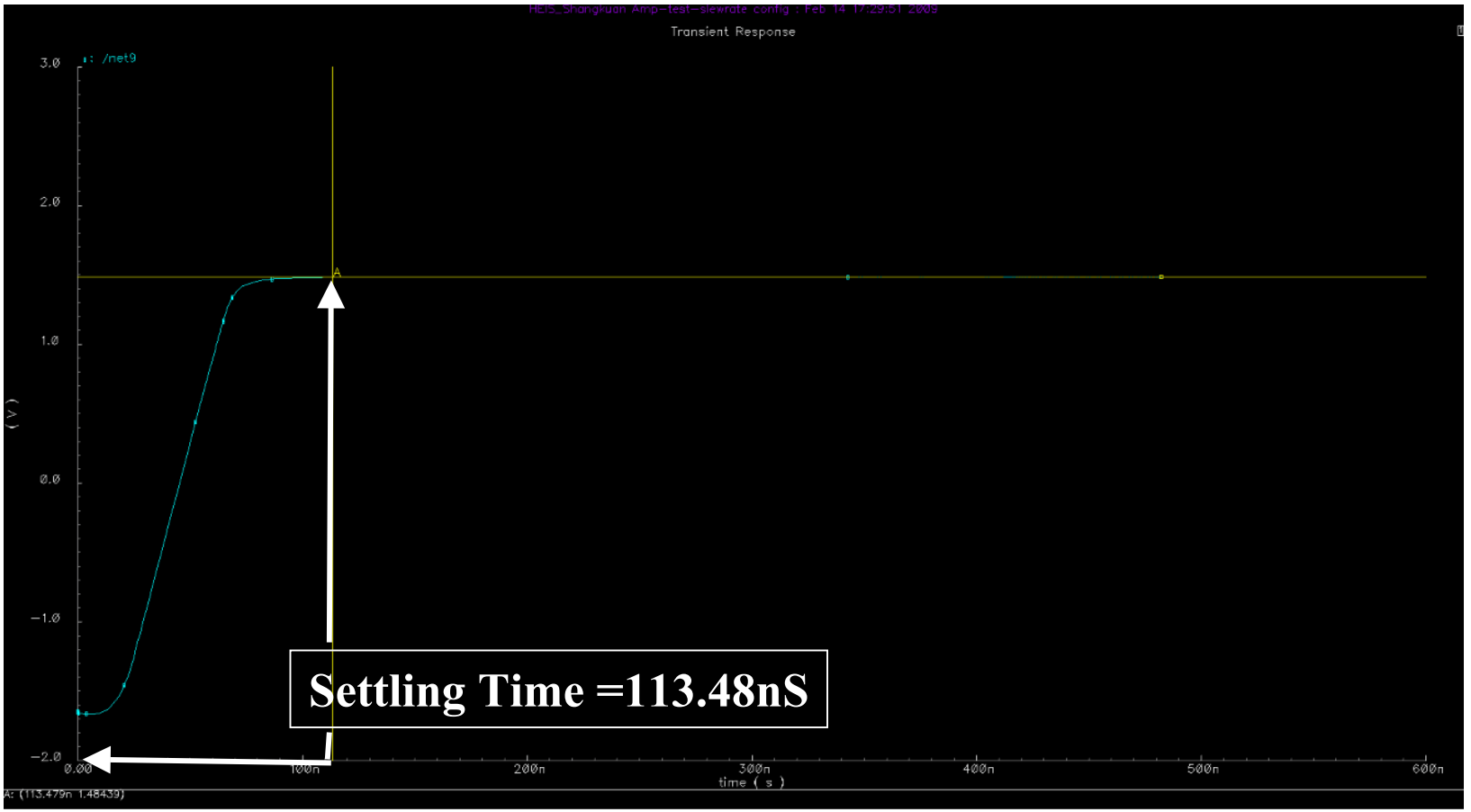
OpAmp Post Layout Simulation

Slew Rate



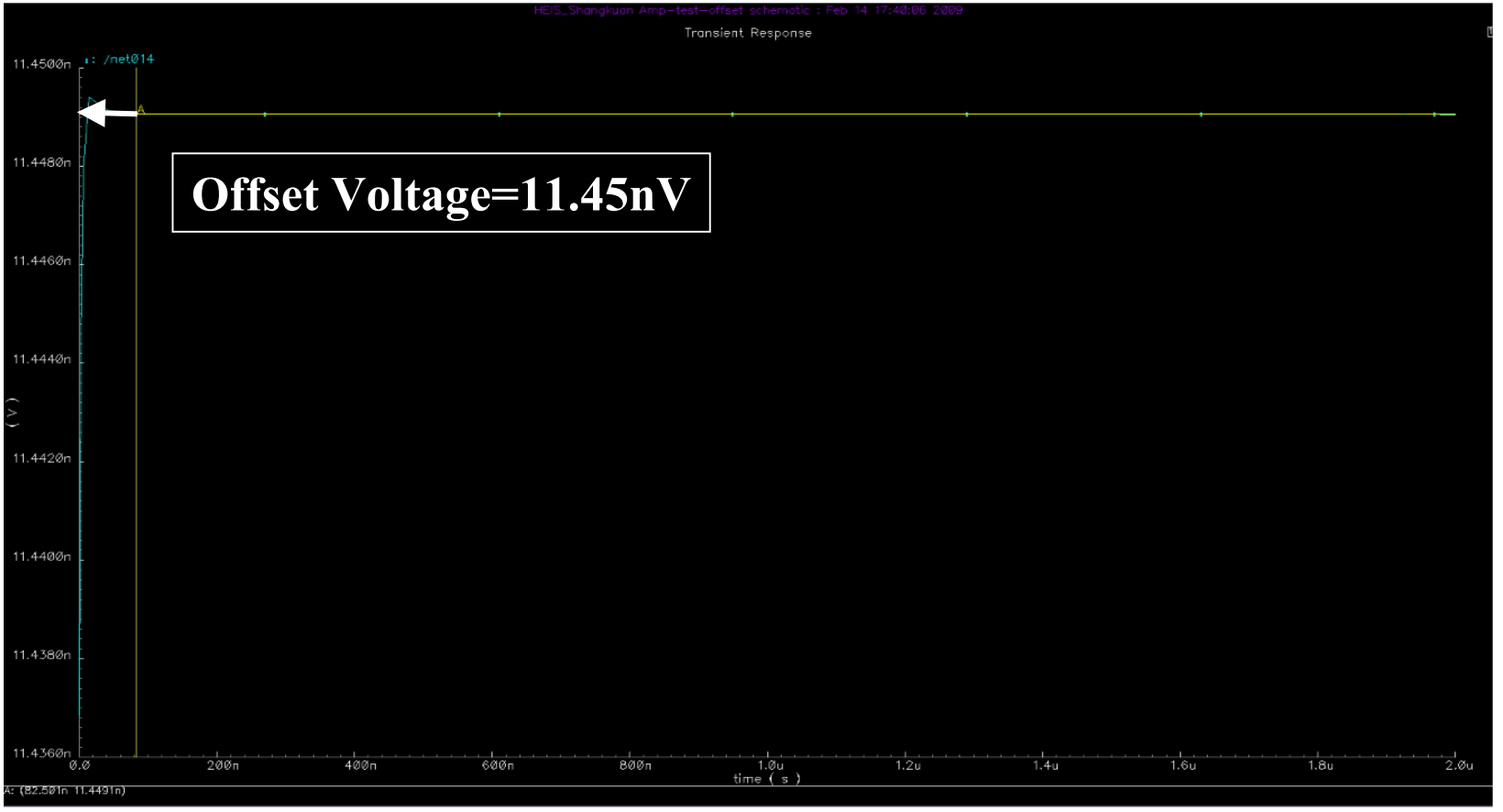
OpAmp Post Layout Simulation

Settling Time



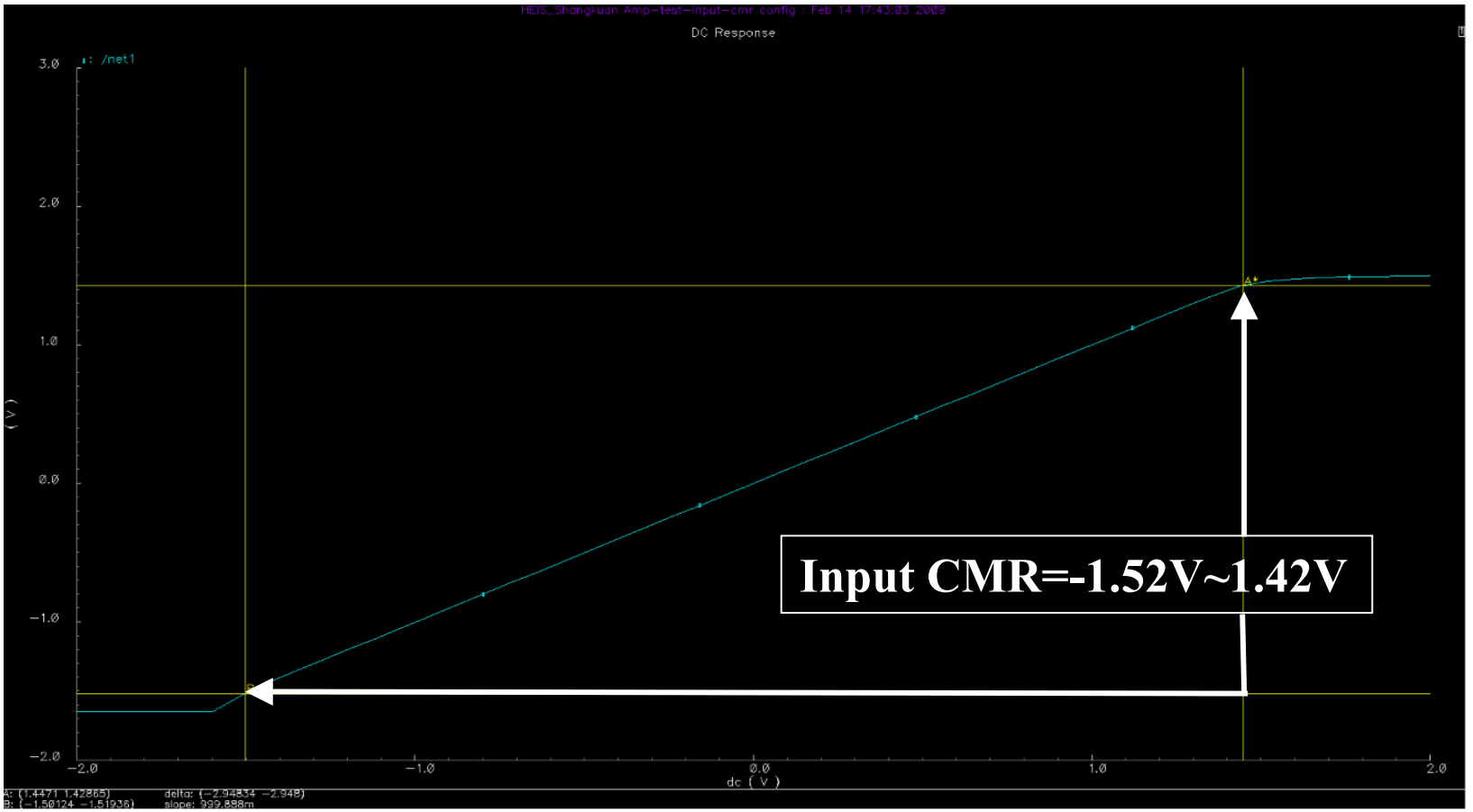
OpAmp Post Layout Simulation

Offset Voltage



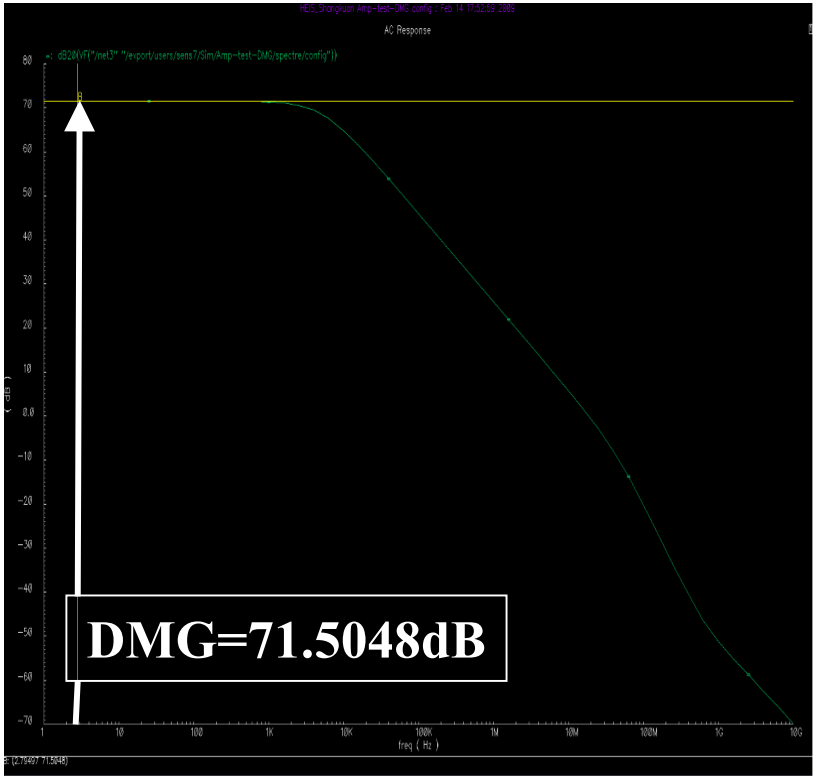
OpAmp Post Layout Simulation

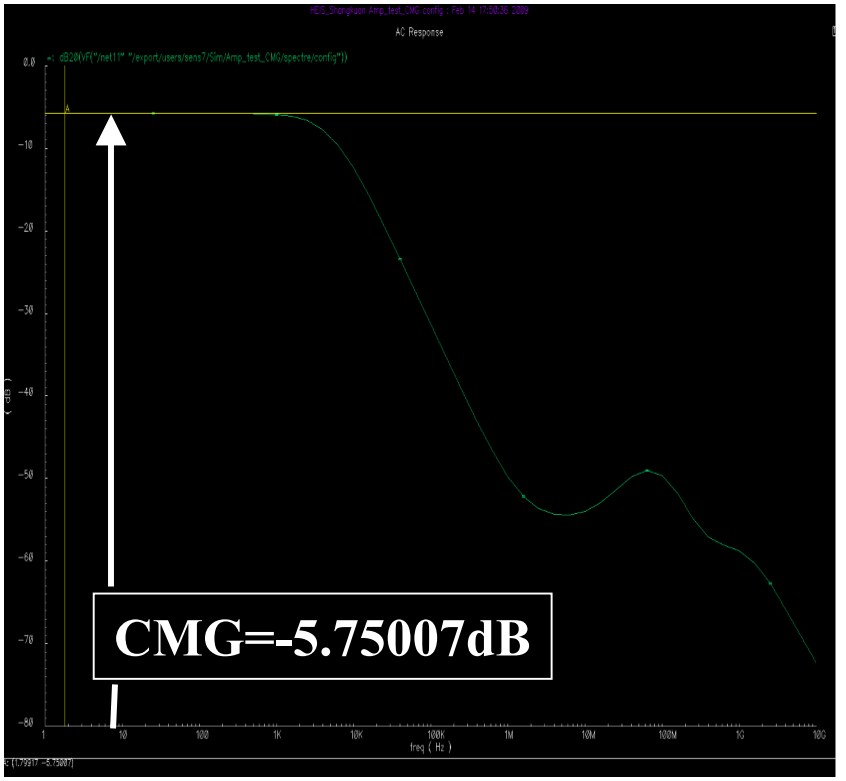
Input CMR



OpAmp Post Layout Simulation

CMRR

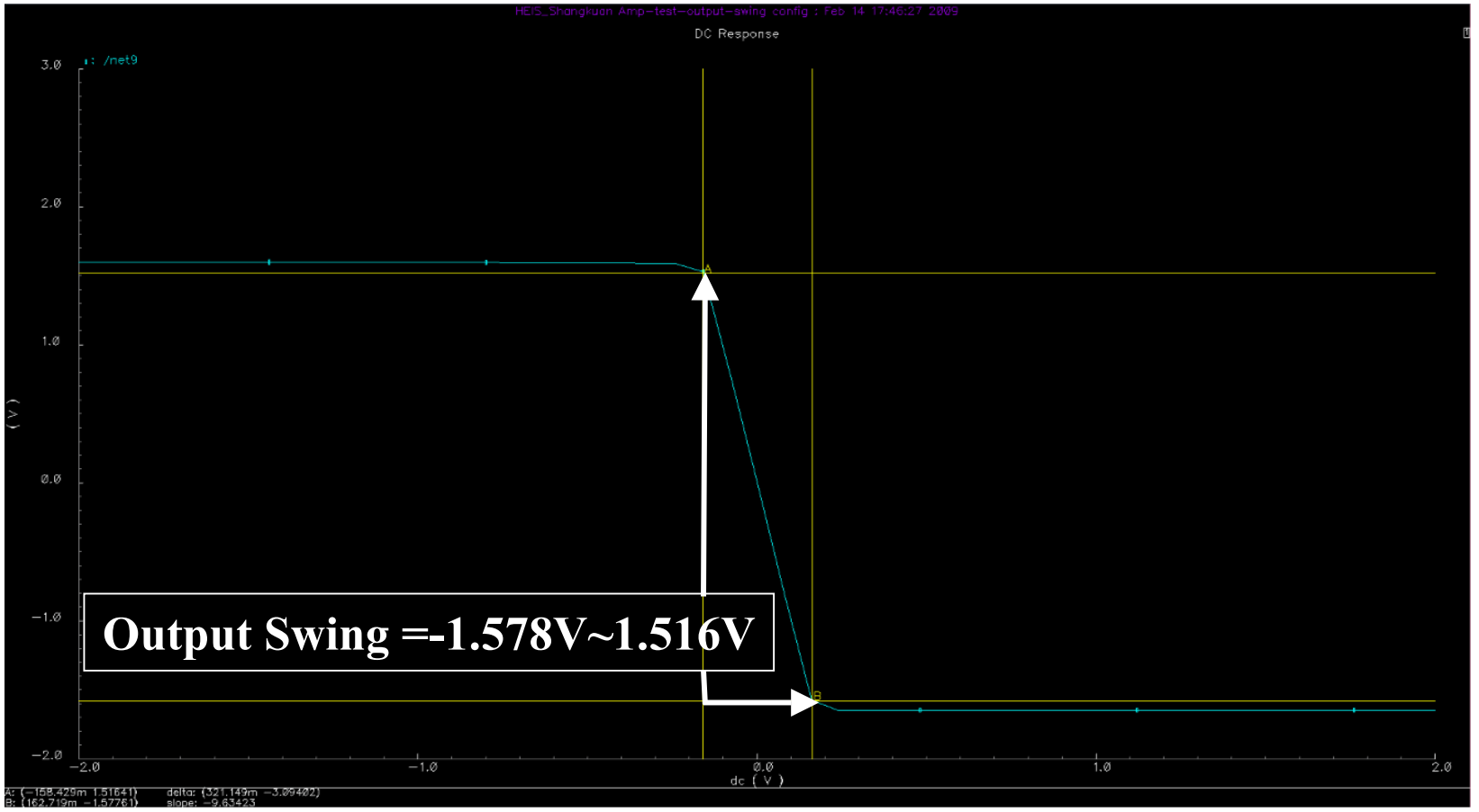




- **differential mode gain**
  CMRR = (differential-mode gain) – (common-mode gain)
- **common mode gain**

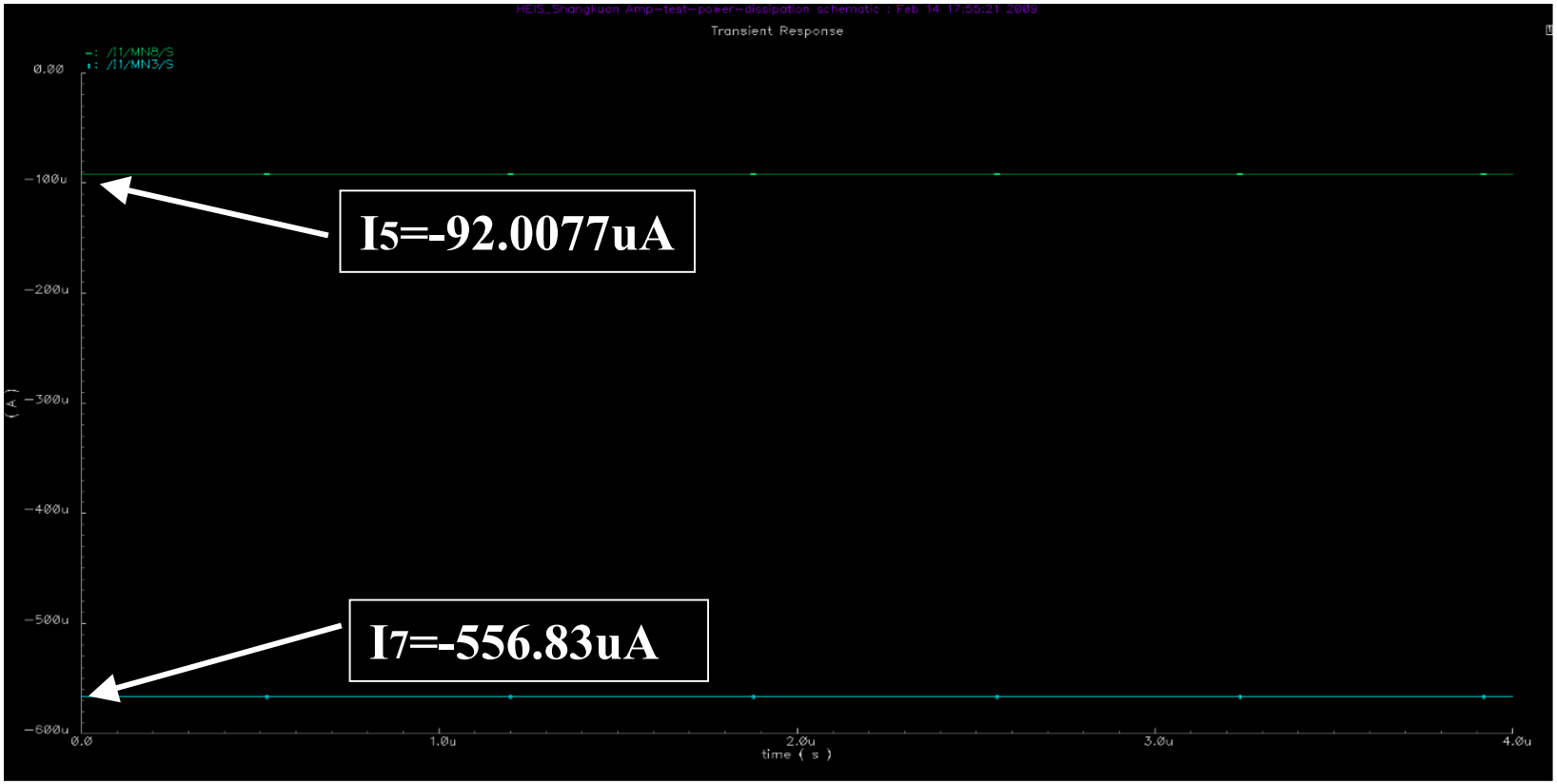
OpAmp Simulation

Output Swing



OpAmp Simulation

Power Dissipation



$$P_{diss} = 3.3V \cdot I_{diss}$$

Results

	Targeted values	Design Plan	Schematic	Analog-extracted
Open Loop Gain	> 70 dB	67.84dB	72.6 dB	72.44 dB
Gain Bandwidth	10 MHz	4.35MHz	18.97MHz	18.7 MHz
Phase Margin	> 65°	64 °	65.5 °	65 °
Settling Time	< 1 μ s	560.1ns	117.7 ns	113.5 ns
Slew Rate	> 30 V/ μ s	10V/ μ s	60.85V/ μ s	60.37V/ μ s
Offset Voltage	< 10 μV	98.21nV	11. 43nV	11.45nV
Input CMR	+/- 1 V	-1.642 V-1.52V	-1.54V~1.42V	-1.51V~1.43V
Output Swing	+/- 1 V	-1.538V~1.555V	-1.58V~1.52V	-1.58V~1.52V
CMRR	> 80 dB	88.03dB	77.1dB	77.3 dB
Power Dissipation	minimum	1.72mW	2.13mW	2.14mW

	s1	s2	s3	s4	s5	s6	s7	Cc
Caculated size (W/L)	1	1	6	6	2	40	7	1.1pF
Analog_extracted size (W/L)	4	4	12.5	12.5	16	150.2	95.2	1.5pF

Conclusion

- This design mainly focus on the high speed application ,so the slew rate and settling time are critical. other specifications eg:Input CMR, Output Swing sequentially get a desirable valuewhen the circuit is finally adjusted and optimaized

- In the design the power dissipation is relatively high ,while I use large transistors ,eg:M_5,M_7 in order to get desiable specifications with high speed application.

- In the design plan I try to get phase margin around 70 °,but the trade off between slew rate and phase margin mainly depends on the compensition capcitance. Finally the Phase Margin is 65 °,and slew rate is 60.37V/ μ s.

The End